REMARKS

The Decision from Appeal dated July 31, 2008 has been received and carefully noted. The enclosed Request for Continued Examination (RCE), the above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1-12 and 14-23 have been amended to more particularly point out and distinctly claim the subject matter of the invention. The independent claims have been amended, in part, to recite the feature of selecting a data rate for transferring data between the apparatus and further apparatus over a plurality of channels. Support for the claim amendments may be found at least in paragraphs 0035-0039 of the specification. Claim 13 has been canceled without prejudice or disclaimer. No new matter has been added. Claims 1-12 and 14-23 are respectfully submitted for consideration.

The final Office Action dated June 20, 2006 rejected claims 1, 18, and 23 under 35 U.S.C. §102(a) as being anticipated by Sadjadpour (U.S. Publication No. 2001/0055332). Applicants submit that claims 1, 18 and 23 recite subject matter which is neither disclosed nor suggested by Sadjadpour, as will be discussed below.

Claim 1, upon which claims 2-17 are dependent, recites an apparatus including bit rate selecting circuitry configured to select a data rate for transferring data between the apparatus and a further apparatus over a plurality of channels. The apparatus further includes modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences, and circuitry configured to determine a power allocation for at

least one bit loading sequence based on minimizing an error rate for the data rate. The apparatus also includes circuitry configured to select a bit loading sequence from the set of bit loading sequences with a lowest error rate for the data rate.

Claim 18 recites a method including selecting a data rate for transferring data between an apparatus and a further apparatus over a plurality of channels, and identifying a set of bit loading sequences from a plurality of modulation alphabets. The method further includes determining a power allocation for at least one bit loading sequence based on minimizing an error rate for the data rate, and selecting a bit loading sequence from the set of bit loading sequences with a lowest error rate for the data rate and applying the power allocation to at least one communication channel.

Claim 23 recites an apparatus including selecting means for selecting a data rate for transferring data between an apparatus and a further apparatus, and providing means for providing a modulation circuitry having a plurality of modulation alphabets and for providing a set of bit loading sequences. The apparatus also includes determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate for the data rate, and selecting means for selecting a bit loading sequence from the set of bit loading sequences with a lowest error rate for the data rate.

As will be discussed below, Sadjadpour fails to disclose or suggest all of the elements of the claims, and therefore fails to provide the advantages and features discussed above.

Sadjadpour discloses a discrete multi-tone modem that operates to minimize cross talk over a twisted pair cable. The spectrum of the twisted pair cable can be split into multiple sub-bands or QAM channels, where each channel is able to handle K_i bits of data, where i is the member of the channel (Sadjadpour, paragraph 0027). The bit addition algorithm of Sadjadpour describes how an array of different bit allocation settings are ordered in ascending order so that bit allocation can be determined based on the least possible power for the maximum data rate possible or a desired data rate (Sadjadpour, 0037-0038). Bits are then added and the process continued until the addition of any further bit in any of the frequency bins violates at least one predetermined constraint, such as power budget, power mask, or maximum number of bits per frame, for example. Further, in another described embodiment of Sadjadpour, the method of allocating bits is modified by modifying the incremental power term by a weighting dependent on the frequency of the tone (sub-frequency). The effect of this weighting function forces the algorithm towards the lower frequencies, which according to the disclosure, has the effect or goal of reducing the near end cross talk (NEXT) power.

Applicants respectfully submit that Sadjadpour fails to disclose or suggest all of the elements of claims 1, 18 and 23. For example, Sadjadpour does not disclose or suggest "determining a power allocation for at least one bit loading sequence based on minimizing an error rate for the data rate; and selecting a bit loading sequence from the set of bit loading sequences with a lowest error rate for the data rate," as recited in claim 18 and similarly recited in claims 1 and 23.

Paragraph 0033 of Sadjadpour, for example, discloses that "any algorithm that is based on minimising a weighted combination of the total power and total data rate could utilise the new performance function described in the present application." Thus, a person of ordinary skill in the art would understand that this implication is aimed at optimizing the function described as a weighted combination of the total power and total data rate. Sadjadpour goes on to describe an energy or power required to transmit b_k bits for a QAM constellation arrangement.

Paragraphs 0034 and 0035 of Sadjadpour discuss the power needed to transmit one additional bit or power saved by removing one bit from a specific frequency bin k. As would be understood by a person of ordinary skill in the art having read the previous part of the description, the system operates by having a number of frequency bins, each of which then sends a QAM transmission. Therefore, according to Sadjadpour, each frequency bin may have a different QAM constellation arrangement according to the method of selection disclosed.

Paragraph 0036 of Sadjadpour goes on to describe a simplification of the power function shown in equation 2 by simplifying it as being a function of the noise power N_k, the coding gain for the frequency g_k and then a factor which is dependent on the parameters bit error rate BER and the number of bits b. This function S(BER,b) is a signal to noise ratio dependent value.

Paragraph 0037 of Sadjadpour then describes two expressions which represent the increment in power needed for a bit addition algorithm and a decrement in power

obtained in a bit removal algorithm. Sadjadpour further discloses that the bit addition algorithm and bit removal algorithm in paragraph 0038 describes how the array of addition and decrement values are sorted in order and a bit added to the frequency bin that requires the least increment in power. The power needed for increasing the number of bits by one bit in the frequency bin, to which it is added in a step is then recalculated and the array is re-sorted. Bit allocation is determined based on the array such as the bit allocation to the frequency bins requires at least a possible power for the maximum possible for the desired bit data rate.

Nowhere within these sections of Sadjadpour is it described that the bit error rate is used as a further determinant and could be considered to be simply a selected value. For example, the algorithm could work by selecting a specific error rate for which the algorithm calculates the array of incremental and decremental values which are then sorted.

Paragraphs 0039-0042 of Sadjadpour then describe a separate embodiment where the minimized near external cross taught factor could also be minimized. This option is shown later in paragraph 0044 by the function 67 which is described as "function 67, a shaded block, representing the minimization of the total cross talk (NEXT) power for a given data rate." Paragraph 0044 does disclose that as a system, there is a series of function blocks. The function blocks are, as described in paragraph 0043, in two forms, the clear blocks that exist in the literature and the new objective functions represented by shaded blocks. The shaded blocks, for example, block 61 representing the joint

minimization of the NEXT and maximization of the total data rate, function 64 representing the joint minimization of an arbitrary function of the total power and the maximization of the total data rate, and function 67 representing the minimization of the total cross talk for a given data rate are those described previously. Furthermore, it is disclosed that function 62, which represents a joint minimization of the bit error rate and maximization of the total data rate, is one of several functions which "exist in the literature".

Therefore, Applicants submit that Sadjadpour does not provide any disclosure or suggestion of making a determination of a power allocation for at least one bit loading sequence based on minimizing an error rate for the data rate, or of selecting a bit loading sequence from the set of bit loading sequences with a lowest error rate for the data rate.

Although Sadjadpour may disclose a method for selecting a bit loading sequence to minimize power consumption, as indicated in paragraphs 0037 and 0038, or a bit allocation algorithm to minimize the cross talk power, as indicated in paragraph 39 to 41, there is no direct or unambiguous disclosure of a determination of the power allocation for at least one bit loading sequence based on minimizing an error rate for a data rate, only the passing comment that there is a "function representing the joint minimization of the bit error rate and maximization of the total data rate".

Although the Office Action appears to have taken the position that the process of Figure 6 of Sadjadpour effectively selects a bit loading sequence with a lowest error rate

for that particular data rate. There is no clear direct and unambiguous disclosure of such, only of a joint minimization of the bit error rate and maximization of the total data rate.

According to embodiments of the claimed invention, on the other hand, a power allocation for at least one bit loading sequence is determined based on minimizing an error rate for the data rate, and a bit loading sequence from the set of bit loading sequences is selected with a lowest error rate for the data rate.

Sadjadpour only discloses a wish for a joint minimization of the bit error rate and maximization of the total data rate at the best, and fails to teach how this wish is further applied to the selection of a bit loading sequence with a lowest error rate for the data rate, or of a power allocation for the same.

Thus, Applicants respectfully assert that Sadjadpour fails to disclose or suggest, at least, "determining a power allocation for at least one bit loading sequence based on minimizing an error rate for the data rate; and selecting a bit loading sequence from the set of bit loading sequences with a lowest error rate for the data rate," as recited in claim 18 and similarly recited in claims 1 and 23. Accordingly, Applicants respectfully assert that the rejection of claims 1, 18 and 23 be withdrawn.

Claims 2-13, 19, 20, and 22 were rejected under 35 USC §103(a) as being unpatentable over Sadjadpour, in view of Applicants' admitted prior art shown in Figures 1 and 2 of the application (AAPA). The Office Action took the position that Sadjadpour disclosed all the elements of the claims, with the exception of a MIMO system. The

AAPA was cited as allegedly curing the deficiencies in Sadjadpour. This rejection is respectfully traversed for at least the following reasons.

Claim 19 recites an apparatus including first circuitry configured to decompose a communication channel between the apparatus and a further apparatus into a plurality of logical channels, and bit rate selecting circuitry configured to select a data rate for transferring over the communication channel. The apparatus further includes modulation circuitry having a plurality of modulation alphabets, wherein at least two modulation alphabets are capable of representing data using a different number of bits so that for the selected data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels. The apparatus also includes second circuitry configured to allocate a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences for the data rate, and third circuitry configured to choose a bit loading sequence from the set of bit loading sequences having a minimum bit error rate for the data rate.

Claim 20, upon which claim 21 is dependent, recites a method including selecting a data rate for transferring data between an apparatus and a further apparatus over a communication channel, and decomposing the communication channel into a plurality of logical channels. The method further includes selecting from a plurality of modulation alphabets, wherein at least two modulation alphabets for modulating data are capable of representing the data using a different number of bits, and identifying a set of bit loading sequences for the selected data rate which specify a number of bits to be loaded onto

corresponding logical channels of the plurality of channels. The method also includes allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences for the data rate, and choosing a bit loading sequence from the set of bit loading sequences having a minimum bit error rate for the data rate.

Claim 22 recites an apparatus including rate selecting means for selecting a data rate for transferring data over the communication channel, and decomposing means for decomposing a communication channel into a plurality of logical channels. The apparatus also includes representing means for representing data using a different number of bits so that for the selected data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels, and allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences for the data rate. The apparatus further includes choosing means for choosing a bit loading sequence from the set of bit loading sequences having a minimum bit error rate for the data rate.

As will be discussed below, the combination of Sadjadpour and AAPA fails to disclose or suggest all of the elements of the claims, and therefore fails to provide the advantages and features discussed above.

Sadjadpour is outlined above. AAPA can be found in paragraphs 0005-0023 of the specification.

Applicants submit that the combination of Sadjadpour and AAPA does not disclose or suggest all of the elements of claims 19, 20 and 22. For example, the combination of Sadjadpour and AAPA fails to disclose or suggest "allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences for the data rate, and choosing a bit loading sequence from the set of bit loading sequences having a minimum bit error rate for the data rate," as recited in claim 20 and similarly recited in claims 19 and 22.

As discussed above, Sadjadpour merely discloses a joint minimization of the bit error rate and maximization of the total data rate. Sadjadpour does not disclose allocating a power weighting for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences for the data rate, and choosing a bit loading sequence from the set of bit loading sequences having a minimum bit error rate for the data rate. AAPA fails to cure these deficiencies in Sadjadpour. Thus, the combination of Sadjadpour and AAPA fails to disclose or suggest all of the elements of claims 19, 20 and 22.

Claims 2-13 are dependent upon claim 1 and inherit all of the limitations thereof. As outlined above, Sadjadpour fails to disclose or suggest all of the limitations of claim 1. AAPA does not cure these deficiencies in Sadjadpour, as AAPA also fails to disclose or suggest determining a power allocation for at least one bit loading sequence based on minimizing an error rate for the data rate and selecting a bit loading sequence from the set

of bit loading sequences with a lowest error rate for the data rate. Thus, the combination of Sadjadpour and AAPA fails to disclose or suggest all of the elements of claims 2-13. Furthermore, claims 2-13 should be allowed for at least their dependence upon claim 1, and for the specific limitations recited therein.

Claims 14-17, and 21 were rejected under 35 USC 103(a) as being obvious over Sadjadpour, in view of AAPA, and further in view of Kim (U.S. Patent Publication No. 2003/0128769). In making this rejection, the Office Action took the position that Sadjadpour disclosed all the elements of the invention except for codings and modulations that utilize system bits. The AAPA and Kim were cited as curing the deficiencies in Sadjadpour. This rejection is respectfully traversed for at least the following reasons.

Sadjadpour and AAPA are discussed above. Kim discloses a method for providing first and second interleaved bit streams to a modulator in order to transmit the first and second interleaved bit streams through at least two antennas in a mobile communication system. An encoder encodes a transmission data stream into a first bit stream with first priority and a second bit stream with second priority being lower than the first priority. An interleaver interleaves the first and second bit streams into the first and second interleaved bit streams. The modulator modulates the first and second interleaved bit streams.

Claims 14-17 and 21 are dependent upon claims 1 and 20, respectively. As discussed above, the combination of Sadjadpour and AAPA fails to disclose or suggest

all of the elements of claims 1 and 20. Additionally, Kim does not cure the deficiencies in Sadjadpour and AAPA, as Kim also fails to disclose or suggest determining a power allocation for at least one bit loading sequence based on minimizing an error rate for the data rate and selecting a bit loading sequence from the set of bit loading sequences with a lowest error rate for the data rate. Thus, the combination of Sadjadpour, AAPA and Kim fails to disclose or suggest all of the elements of claims 14-17 and 21. Furthermore, claims 14-17 and 21 should be allowed for at least their dependence upon claims 1 and 20, and for the specific limitations recited therein.

For at least the reasons discussed above, Applicants respectfully submit that the cited prior art fails to disclose or suggest all of the elements of the claimed invention. These distinctions are more than sufficient to render the claimed invention unanticipated and unobvious. It is therefore respectfully requested that all of claims 1-12 and 14-23 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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